REMARKS

Claims 1-22 have been canceled without prejudice, waiver, or disclaimer; and claims 23-44 have been added. Therefore, claims 23-44 are now pending in the present application. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Telephone Interviews

Applicants wish to express their appreciation to the Examiner for spending time discussing the present application with the Applicants' representative on April 26th and April 27th. During these discussions, the Examiner seemed to indicate that certain amendments to the claims should be made to resolve many of the issues that have arisen during prosecution. Claim amendment proposals were discussed in an attempt to resolve these issues and to follow the Examiner's suggestions. In this respect, Applicants request that the Examiner kindly consider the claim amendments submitted herein.

II. Response to 35 U.S.C. §102 Rejection

Claims 1, 6-11, 14, and 21 were rejected under 35 U.S.C. §102(b) as being anticipated by *Chakradhar et al.* (U.S. Patent No. 5,726,996). Since these claims have been canceled by amendment herein, the rejection is now considered to be moot.

A. Claim 23

Newly-added independent claim 23 is directed to a method for testing an integrated circuit. The method comprises, *inter alia*, generating a test vector, assigning values to a portion of the bits of the test vector to detect at least one target fault, and marking the at least one target fault as detected. The generating, assigning, and marking are repeated ***"until all target faults...are marked."*** A remainder of the bits of the test vectors are left as unspecified bits. The method further comprises ***"non-randomly filling a plurality of the unspecified bits for each test vector with values that enable each test vector to be compressed"*** and ***"compressing each test vector to create a compressed vector having fewer bits."***

Applicants assert that the combination of features highlighted above are not taught or disclosed by *Chakradhar et al.* or the other prior art references of record.

The claimed method includes generating, assigning, and marking until all target faults are marked. It should be noted that, independent of detecting all target faults, the method further includes non-randomly filling unspecified bits. Thus, non-randomly filling does not contribute to detecting the faults, but instead is performed to enable each test vector to be compressed. As mentioned in an earlier response, compression is not the same concept as compaction, which involves combining two test vectors into one. Rather, compression, as defined in the claim, is consistent with its ordinary meaning in the art such that compressing each test vector consequently creates a compressed vector having fewer bits.

It is believed that the prior art references do not teach or disclose filling test vectors in such a way as to enable compression and then compressing the test vectors, such that this filling and compressing are performed independent of the detection of faults. For at least these reasons, Applicants contend that claim 23 is allowable over the prior art of record and respectfully requests that the 35 U.S.C. §102 rejection be withdrawn.

B. Claim 36

Independent claim 36 is directed to an apparatus for generating a set of test vectors. The apparatus comprises, *inter alia*, means for generating a test vector, means for assigning values to a fraction of the bits of the test vector to detect at least one target fault, and means for marking the at least one target fault as detected. The assigning is performed ***"until all target faults are detected."*** A remainder of the bits of the test vectors are left as unspecified bits. The apparatus further comprises ***"means for non-randomly filling a plurality of the unspecified bits for each test vector with values that enable each test vector to be compressed"*** and ***"means for compressing each test vector to create a compressed vector having fewer bits."***

Applicants assert that the combination of features highlighted above are not taught or disclosed by the prior art of record. It is noted, for example, that the claimed apparatus includes means for generating, means for assigning, and means for marking, which operate until all target faults are detected. Independent of detecting all target faults, the apparatus further includes means for non-randomly filling unspecified bits. Therefore, the means for non-randomly filling does not contribute to the detection of faults, but instead includes the function of filling the unspecified bits with values that

enable each test vector to be compressed. Again, compression is not the same concept as compaction, which involves combining two test vectors into one. Rather, the means for compressing, as defined in the claim, operates to compress each test vector so as to create a compressed vector having fewer bits.

It is believed that the prior art references do not teach or disclose means for non-randomly filling test vectors in such a way as to enable compression and mean for compressing the test vectors, such that the means for filling and means for compressing function independently of the detection of faults. For at least these reasons, Applicants contend that claim 36 is also allowable over the prior art of record.

C. **Claim 41**

Independent claim 41 is directed to an ATPG for testing an integrated circuit for a list of faults. The ATPG comprises, *inter alia*, logic for generating a set of test vectors and logic for assigning values to a number of bits for each test vector and continuing to assign values to the bits ***"until all target faults...are detected."*** A remainder of the bits of each test vector are left as unspecified bit positions. The ATPG further comprises ***"logic for non-randomly filling a plurality of the unspecified bit positions for each test vector after the logic for assigning has assigned values to detect all target faults, the logic for non-randomly filling thereby enabling each test vector to be compressed"*** and ***"logic for compressing each test vector to create a compressed vector having fewer bits."***

Applicants assert that the combination of features highlighted above are not taught or disclosed by the prior art of record. For example, the claimed ATPG includes logic for generating and logic for assigning values until all target faults are detected, and, independent of detecting all target faults, the ATPG further includes logic for non-randomly filling unspecified bits. Therefore, the logic for non-randomly filling does not contribute to the detection of faults and is performed after the logic for assigning has assigned values to detect all target faults. Instead, the logic for non-randomly filling operates to enable each test vector to be compressed. Again, compression is not the same concept as compaction, but is consistent with its ordinary meaning in the art such that the logic for compressing each test vector consequently creates a compressed vector having fewer bits.

It is believed that the prior art references do not teach or disclose ATPG having logic for filling test vectors in such a way as to enable compression and logic for actually compressing the test vectors, in which the logic for filling and the logic for compressing are performed independent of the detection of faults. For at least these reasons, Applicants contend that claim 41 is also allowable over the prior art of record and respectfully requests that the 35 U.S.C. §102 rejection be withdrawn.

D. Claims 24-35, 37-40, and 42-44

Dependent claims 24-35, 37-40, and 42-44 are believed to be allowable for at least the reason that these claims depend from allowable independent claims 23, 36, and 43.

III. Response to 35 U.S.C. §103 Rejection

Claims 2-5, 12, 13, 15-20, and 22 were rejected under 35 U.S.C. §103 as being unpatentable over *Chakradhar et al.* (U.S. Patent No. 5,726,996). Since these claims have been canceled, this rejection has been rendered moot.

The independent claims are believed to be allowable for at least the reasons that the prior art does not teach or suggest each and every feature of the claims, as mentioned above. In addition, Applicants assert that, not only does the prior art fail to teach or suggest all the features of the claims, but the prior art also fails to provide any motivation or suggestion to combine reference teachings in such a way as to read on the claims. In this regard, Applicants respectfully contend that the claims are in condition for allowance and that the claims, as amended, are non-obvious with respect to the prior art. Withdrawal of the 35 U.S.C. §103 rejection is therefore respectfully requested.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been rendered moot and/or accommodated, and that the pending claims 23-44 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 5-5-04

Evelyn Sanders
Signature – Evelyn Sanders